Analysis of DC Fault for Dual Active Bridge DC/DC Converter including Prototype Verification

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Abstract

This paper presents DC fault analysis for a dual active bridge DC/DC converter which comprises of two active bridges and an internal medium frequency transformer. This topology provides galvanic isolation, voltage step up/down and bidirectional power transfer. The DC fault study assumes the DC terminal voltage of the converter is at zero. The steady state fault current is limited to a low magnitude which is less than the rated value without any controller action depending on the design of the converter. The DC faults current magnitudes are analyzed with AC equivalent circuit where only the fundamental component of the AC voltages and inductor current are considered. Phase shift and AC voltage magnitude modulation control methods are selected. A detailed dual active bridge DC/DC converter 3 MW, 4/40 kV based system is simulated using MATLAB/Simulink to validate the proposed analytical study. Further, hardware testing is conducted to confirm the DC fault studies with a 500 W 24/100 V prototype.

Keywords—Dual active bridge (DAB), DC terminal fault, High power application

I. INTRODUCTION

The recently proposed DC grids place a high possibility for DC/DC converter technology to be used for power exchange and voltage stepping. These are to facilitate the transnational DC grids between countries to integrate the large number of renewable energy generation especially the planned offshore wind farms to be installed in the North Sea. DC has major disadvantage concerning protection that raised issue on its reliability. Today, the feasibility of DC grids relates to two key high power components, 1) DC circuit breaker (CB) and 2) DC transformer [1-3]. The DC CB is required to isolate faulted DC line and the DC transformer is used to convert voltage levels according to the DC grid voltage level.

The traditional circuit breakers are unable to switch large DC fault currents caused by the lack of inductances in DC grids. Therefore, the fault current is only limited by the resistance of the DC cables. This fault current needs to be suppressed quickly to avoid aggravation which can consequently damage components and give high repair/replacement costs especially in offshore installation. The isolation of faults in DC grids is difficult compared to AC grids because of several disadvantages: no zero crossings of DC current, converter system is prone to overvoltages and overcurrents when interrupting high fault current, high peak current during fault requires high device ratings and costs, zero/low inductance in the DC links where only small resistance from DC cables limiting the fault current [1, 4-5]. DC circuit breaker concepts are available in literatures that are mainly categories into four types [3, 5-7].

The dual active bridge (DAB) DC/DC converter is one of the attractive solutions for DC grid applications and is often used for bidirectional power transfer [8]. It is known for its high power density, symmetrical structure, voltage step up/down, bidirectional power flow and zero voltage switching (ZVS) capability. However, there are no analytical studies on DC faults current magnitude for this type of converter. In DC grid applications, operating the DAB transformer at medium frequency (MF) can significantly reduce the size and weight of the AC transformer. The resulting impedance of the transformer can only limit fault current to a certain value. This fault current can damage the power switches, saturate the

transformer core and deteriorate the converter operation. The saturation may cause the non-zero average flux in the transformer core which gives DC offset to the converter AC waveforms [9]. It can be overcome by controlling the DC offset to zero or designing the transformer at an appropriate operating flux density. Authors in [9] have demonstrated that this DC offset can be controlled by phase shift (PS) angle control. Another method to overcome DC offset is to connect two coupling capacitor in series with the primary and secondary windings [10] but this method uses additional passive device in the AC circuit which can cause additional failure to the converter. The authors in [10] also addressed the DAB converter performance when a fault happened in the switches. This type of fault in switches may either open or short the circuit. If short, the fault is going to be similar to pole to ground fault (unsymmetrical fault).

The operation of a DAB DC/DC converter operation in DC grid is critical to operate continuously to supply power and withstand event such as DC link fault. During fault, one of the bridges that see the DC fault becomes a diode rectifier. The other active bridge of the converter can be used to control the fault current. The authors in [10-11] proposed rapid fault detection by monitoring sudden changes in the AC voltages and use this information to turn off the gate signals to the switches. The fault ride through method is integrated in the control by setting the saturation limit of maximum current reference. In [12], similar investigation as [10] was carried out by detecting the AC voltage of the converter but the authors use four-step open circuit diagnosis to trigger an active phase shift control system to locate the fault. For multi-terminal DC application, the authors in [13] proposed handshaking method to locate and isolate faulted DC line without any communication. However, the method reliability depends on the exchanges of information which is known to have delay in transferring of data. Although, power switch failure in the DAB converter bridge has been addressed in [10], the DC terminal fault analysis is incomplete in the literature such as the effect of DC fault on one of the bridges and the fault current magnitude of the converter. Fault is briefly mentioned in [8] when one bridge is operating with PS control and the other bridge is in diode mode but there is no analysis conducted on DC fault currents. Most work on fault is more on prevention methods and

no derivation of fault current magnitude exists in [11-13]. It is vital to know the converter parameters during fault to get the information to better the converter performance and its operation.

This paper contributes to the DAB converter performance during DC faults when severe fault conditions (pole to pole) is assumed. The aim of the work is to provide derivation of the DAB converter current magnitudes to provide indication and to analyse the converter performance during DC faults. The derived fault current magnitude is expected to be much less than the rated current. The approach of the work is adapted from the work in [14]. Literature [14] provides fault studies for a transformerless LCL DAB converter. A 3 MW 4/40 kV DAB DC/DC converter modeled in MATLAB/Simulink is used to test the converter performance during DC fault and a 500 W24/100V prototype is realised to validate the study.

II. DUAL ACTIVE BRIDGE DC/DC CONVERTER TOPOLOGY

A. *Basic Operation*

A single phase DAB DC/DC converter topology is shown in Fig. 1. It is assumed from this point that the power in the analysis is flowing in one direction (step up mode), from bridge 1 (LV) to bridge 2 (HV). The topology has one bridge working as a DC/AC converter feeding a MF transformer, which then supplies a second bridge working as an AC/DC converter. Each bridge is implemented by power switches S_1-S_4 (bridge 1) and S_5-S_8 (bridge 2). The power switches used are IGBT switches with anti-parallel diodes D_1-D_8. Each bridge can be controlled using its PS angle to control the power flow and level. The AC equivalent circuit of the DAB converter inner circuit is shown in Fig. 2. The parameter L_s is the series inductance, i_L is the inductor current and $n = n_2/n_1$ is the transformer turns ratio.

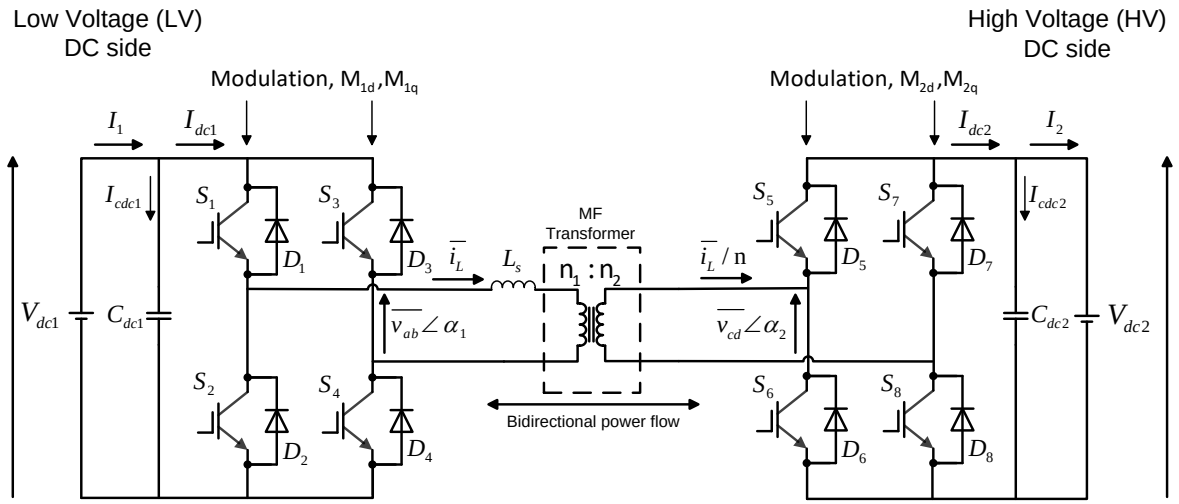


Fig. 1. DAB DC/DC converter topology

B. Circuit Equations

In the analysis, only the fundamental AC component of the square wave AC voltage is used (v_{ab}, v_{cd} variables in Fig. 1 is renamed to v_{ac1}, v_{ac2} in Fig. 2, respectively). The transformer HV side parameters are referred to the LV side. For simplicity, no losses are considered in the analysis. Also, the magnetizing inductance is assumed large enough to not affect the converter operation. The value of the magnetizing inductance is normally large and fixed depending on the core parameters such as its geometry and permeability. The aim of the analysis is focused on DC terminal fault based on the converter steady-state operation.

Referring to Fig. 2, the DAB converter instantaneous AC voltages can be expressed as phasors and its DQ coordinate form as

$$\overline{v_{ac1}} = V_{ac1m}\angle\alpha_1 = V_{ac1d} + jV_{ac1q} \tag{1}$$

$$\overline{v_{ac2}}' = V_{ac2m}'\angle\alpha_2 = V_{ac2d}' + jV_{ac2q}' \tag{2}$$

where $\overline{v_{ac1}}$, $\overline{v_{ac2}}'$ are the phasors of the AC voltages,

V_{ac1m}, V_{ac2m}' are the fundamental AC voltage magnitudes,

α_1, α_2 are the phase shift angle (α_1 is used as the reference coordinate frame),

V_{ac1d}, V_{ac2d}' are the D component of the AC voltages,

V_{ac1q}, V_{ac2q}' are the Q component of the AC voltages.

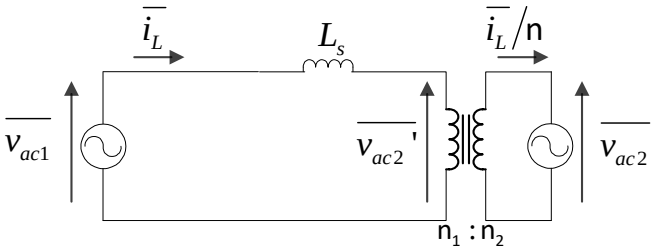


Fig. 2. DAB DC/DC converter AC equivalent circuit

Fig. 3 shows the basic operating waveforms of the DAB converter. From Fig. 3, α_1 and α_2 are the phase angles of LV and HV sides, respectively. The conduction angles γ_1 and γ_2 are the modulation parameters to control the AC voltage magnitudes. The control signals can also be separated into its DQ components and control parameters are introduced as M_{1d}, M_{1q}, M_{2d} and M_{2q} to link the phase angles, α_1 and α_2, and the instantaneous AC voltage. Therefore, the RMS AC voltages are given as

$$\begin{aligned}\overline{v_{ac1}} &= \frac{4V_{dc1}}{\pi\sqrt{2}}\left(\sin\frac{\gamma_1}{2}\cos\alpha_1 + j\sin\frac{\gamma_1}{2}\sin\alpha_1\right)\\ &= V_{ac1m}\left(M_{1m}\cos\alpha_1 + jM_{1m}\sin\alpha_1\right)\\ &= V_{ac1m}\left(M_{1d} + jM_{1q}\right)\end{aligned} \tag{3}$$

$$\begin{aligned}\overline{v_{ac2}}' &= \frac{4V_{dc2}'}{\pi\sqrt{2}}\left(\sin\frac{\gamma_2}{2}\cos\alpha_2 + j\sin\frac{\gamma_2}{2}\sin\alpha_2\right)\\ &= V_{ac2m}'\left(M_{2m}\cos\alpha_2 + jM_{2m}\sin\alpha_2\right)\\ &= V_{ac2m}'\left(M_{2d} + jM_{2q}\right)\end{aligned} \tag{4}$$

where γ_1 and γ_2 are the conduction angles of the switches which equals to M_{1m} and M_{2m} as the modulation magnitude of the switches to control the AC voltage magnitude.

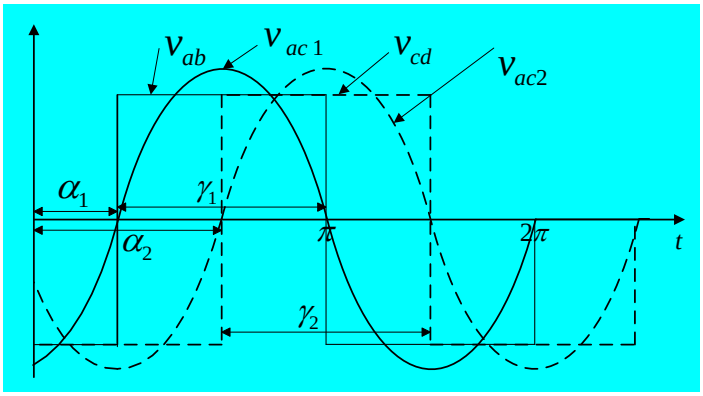


Fig. 3. Basic operating waveform of DAB

Then the steady-state equation for the RMS inductor current can be analyzed with the assumptions when bridge 1 is the referenced voltage (by setting α_1 to zero). Therefore, the LV side AC voltage, $\overline{v_{ac1}}$ in (1) equals $V_{ac1m}=V_{ac1d}$. The RMS inductor current can now be expressed as

$$\bar{i}_L = \frac{V_{ac1d} - (V_{ac2d}' + jV_{ac2q}')}{j\omega L_s} \tag{5}$$

where ω is the angular frequency of the converter.

The RMS inductor current can be expressed as its DQ components as

$$\bar{i}_L = \frac{-V_{ac2q}'}{\omega L_s} + j\frac{(V_{ac2d}' - V_{ac1d})}{\omega L_s} = i_{Ld} + ji_{Lq} = i_{Lm}\angle\theta \tag{6}$$

where i_{Ld} and i_{Lq} are the D and Q component of the inductor current, respectively. i_{Lm} is the magnitude of the inductor current and θ is the inductor current angle.

Eq. (6) is used to calculate the apparent power of the converter at both bridges and can be expressed as

$$\bar{S}_1 = \overline{v_{ac1}}'\bar{i}_L^* = \frac{-V_{ac1d}V_{ac2q}'}{\omega L_s} + j\left(\frac{V_{ac1d}V_{ac2d}' - V_{ac1d}^2}{\omega L_s}\right) \tag{7}$$

$$\overline{S_2} = \overline{v_{ac2}}' \overline{i_L}^* = \frac{-V_{ac1d} V_{ac2q}'}{\omega L_s} + j\left(\frac{V_{ac1d} V_{ac2d}' - V_{ac2d}^2 ' + V_{ac2q}^2 '}{\omega L_s} \right) \quad (8)$$

where the real part of (7) and (8) are the real power and the imaginary part are the reactive power. The negative sign in the real part indicate the power direction from LV to HV side and become positive for power transfer in the opposite direction.

Hence, the real power based on real part of (7) and (8) is assumed similar and can be used to calculate the required L_s such as

$$L_s = \frac{V_{ac1m} M_{1m} V_{ac2m}' M_{2m} \sin(\alpha_2)}{\omega P_2} \quad (9)$$

The designed value of L_s in (9) determines the fault current magnitude of the converter. The DC fault analysis is study in the following section.

III. DC FAULT ANALYSIS

The converter performance is investigated for DC terminal faults to derive the fault current magnitudes. Fig. 4 shows the AC equivalent of the DAB converter during LV and HV terminal faults. The DC fault depends on the power flow direction and on the location of the fault occurrence. This study assumes steady-state operation of the converter and no controller actions are realised.

As an example when there is no control action, the sequence of the DAB converter behaviour during LV side DC terminal fault is as follow:

1) In this case, the converter sees short circuit current at the LV bridge and, the HV bridge feeds this fault current. Therefore, a sort of fault ride through is required to limit the fault current at its rated value. If the fault is permanent, a DC fault detection algorithm shall be implemented to turn off the LV bridge gate signals and becomes diode mode.

2) During fault, the natural transient response of the uncontrolled diode bridge defines its performance until the converter achieves its steady state value.
3) The HV bridge sees this LV side fault current as AC faults and this fault current magnitude is primarily depends on the impedance of the converter.

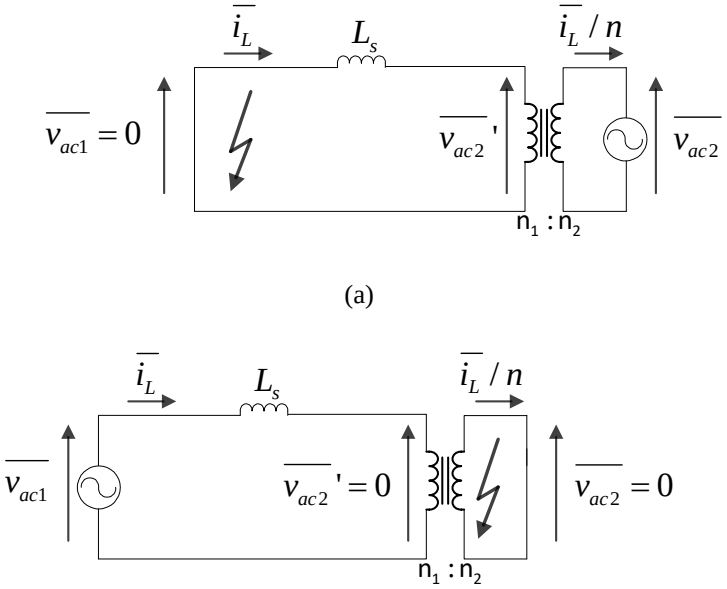


Fig. 4. AC equivalent circuit of the DAB converter during (a) LV DC terminal fault, (b) HV DC terminal fault

On the other hand, similar sequence is expected when DC fault happened at HV side. The converter steady-state inductor current magnitude in (6) is used to investigate the fault current magnitude. The inductor current is at maximum when the converter is assumed to be operating at full power prior to fault (α_2 is at 90˚).

During DC fault, the voltage across L_s only sees one voltage terminal is feeding the fault. At normal operation, the resulting voltage across L_s sees two voltage terminals. This in turn gives higher voltage magnitude across the L_s compared during DC fault. Hence, the inductor current during DC fault will always be in triangular shape (assuming the power switches are operating at full conduction angles).

A. DC fault current magnitude during LV fault

During LV DC side fault conditions (Fig. 4(a)), the DC voltage in (1) is rewritten to

$$\overline{v_{ac1}} = V_{ac1m} = V_{ac1d} = 0 \tag{10}$$

From (6), the converter rated RMS inductor current magnitude during steady state operation is

$$\left|i_{Lrm}\right| = \left|\frac{-V_{ac2q}' + (V_{ac2d}' - V_{ac1d})}{\omega L_s}\right| \tag{11}$$

Using (11), the magnitude of the LV fault current when substituting (10) gives

$$\left|I_{LfmLV}\right| = \left|\frac{-V_{ac2d}' + V_{ac2q}'}{\omega L_s}\right| \tag{12}$$

The magnitude ratio of (12) relative to (11) can be obtained using

$$\left|\frac{I_{Lfm\_LV}}{I_{Lrm}}\right| = \frac{\left|-V_{ac2d}' + V_{ac2q}'\right|}{\left|-V_{ac2q}' + (V_{ac2d}' - V_{ac1d})\right|} \tag{13}$$

Rewriting (13) based on its control signals gives

$$\begin{aligned}\left|\frac{I_{Lfm\_LV}}{I_{Lrm}}\right| &= \frac{\sqrt{-V_{ac2d}^2 + 'V_{ac2q}^2'}}{\sqrt{-V_{ac2q}^2' + (V_{ac2d}^2' - 2V_{ac1d}V_{ac2d}' + V_{ac1d}^2)}} \\ &= \frac{\sqrt{-M_{2d}^2 + M_{2d}^2}}{\sqrt{-M_{2q}^2 + (M_{2d}^2 - 2M_{1d}M_{2d} + M_{1d}^2)}}\end{aligned} \tag{14}$$

Assuming maximum modulation and maximum phase shift angle of 90° (in this case $M_{2d} = 0$, $M_{2q} = 1$), (14) is equal to

$$\left|\frac{I_{Lfm\_LV}}{I_{Lrm}}\right| = \frac{1}{\sqrt{2}} \tag{15}$$

And the peak fault current of (15) is similar to the rated current as

$$\left|I_{Lfm\_LVpk}\right| = \frac{\sqrt{2}\left|I_{Lrm}\right|}{\sqrt{2}} = \left|I_{Lrm}\right| \tag{16}$$

The relationship between the steady-state and fault current based on (15) is given as

$$I_{Lfm\_LV} = 0.707 I_{Lrm} \tag{17}$$

Eq. (17) is only valid if the converter is design to achieve its desired power level at maximum phase shift. If the converter is design say to achieve its desired power at 45° (designing and operating at smaller phase shift angle can reduced the circulating current in DAB converter), (17) becomes $I_{Lfm\_LV} = 1.31 I_{Lrm}$. This is bigger than the rated current value.

Therefore, it is required to set the boundary when the converter fault current exceeds its rated current value. The boundary ratio in (14) is set to two ($I_{Lfm\_LV} = 2I_{Lrm}$). The reason for selecting the limit at two times the rated current is because the power switches can withstand double of its rated value during transient operation which can be happened at the instant DC fault occur [15-16]. However, this operation is limited to the junction temperature of the power switches. The boundary of the converter design of L_s is based on per unit (pu) value. Fig. 5 shows the fault and rated current magnitude ratio calculated using (14) against different series inductance per unit value.

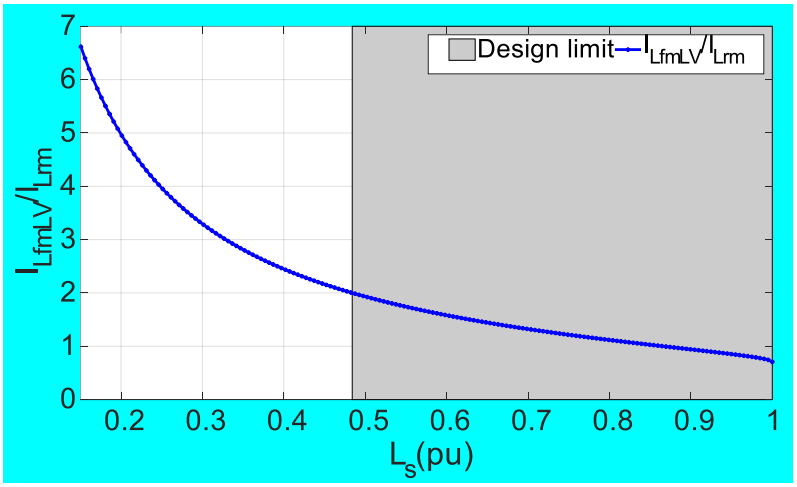


Fig. 5. Fault and rated current magnitude ratio related to the series inductance design

The DAB converter series inductance, L_s boundary within the limit set and the operating phase shift angle to achieve a desired power are

$$\begin{aligned} 0.48\ \text{pu} \le L_s \le 1.0\ \text{pu} \\ 28.96° \le \alpha_2 \le 90° \end{aligned} \tag{18}$$

The boundary of α_2 is calculated using (14) by rewriting the equations based on its sine and cosine functions.

B. DC fault current magnitude during HV fault

On the other hand, during HV side fault (as shown in Fig. 4(b)), the HV DC terminal voltage in (2) becomes

$$\overline{v_{ac2}}' = V_{ac2m}' = 0 \tag{19}$$

Using (11), the magnitude of the AC fault current when substituting (19) is

$$\left| I_{Lfm\_HV} \right| = \left| \frac{V_{ac1d}}{\omega L_s} \right| \tag{20}$$

The magnitude ratio of (20) relative to (11) is

$$\left| \frac{I_{Lfm\_HV}}{I_{Lrm}} \right| = \left| \frac{V_{ac1d}}{-V_{ac2q}' + (V_{ac2d}' - V_{ac1d})} \right| \tag{21}$$

And rewriting (21) to its control signals gives

$$\left| \frac{I_{Lfm\_HV}}{I_{Lrm}} \right| = \frac{\sqrt{V_{ac1d}^2}}{\sqrt{(-V_{ac2q}^2)' + (-V_{ac1d}^2)}} = \frac{M_{1d}}{\sqrt{M_{2q}^2 + M_{1d}^2}} \tag{22}$$

If maximum modulation and maximum phase shift are considered for (22), the relationship between the rated and fault current is similar as (15). From this fault studies, the DAB converter fault current magnitudes primarily depend on the voltage across the inductor. The fault current and rated current magnitudes ratio are

similar for both HV and LV sides. The only difference is because of the transformer turns ratio. The following section shows the plots facilitated using MATLAB for the LV and HV side DC fault studies.

C. *DC fault MATLAB plots*

The DAB converter specification used for the study is given in Table I. The AC fundamental component analysis in this paper is compare with the piecewise linear analysis such as in [8] to determine its accuracy. The power equation in [8] is

$$P_{2lit} = \frac{V_{dc1} n V_{dc2}}{\omega L} \phi \left(1 - \frac{|\phi|}{\pi}\right) \tag{23}$$

where V_{dc1}, V_{dc2} are the voltages at DC terminals, n is the transformer turns ratio, ϕ is the phase shift angle in radian, L is the inductance, P_{2lit} is the required output power and $\omega = 2\pi f$ where f is the converter operating frequency.

TABLE I
SYSTEM PARAMETERS AT RATED VALUE

Parameters	Value
Power, P_1	3 MW
DC voltage at LV, V_{dc1}	4 kV
DC voltage at HV, V_{dc2}	40 kV
Fundamental RMS AC voltage at LV, v_{ac1}	3.6 kV
Fundamental RMS AC voltage at HV, v_{ac2}	36 kV
Average DC current at LV, I_{dc1}	750 A
Average DC current at HV, I_{dc2}	75 A
Fundamental RMS AC current at LV, I_{Lm_LV}	1200 A
Fundamental RMS AC current at HV, I_{Lm_HV}	120 A
Frequency, f	500 Hz

The inductance for this comparison can be calculated based on (9) for fundamental component analysis and based on (23) for piecewise linear analysis. The calculation of the inductance is using the maximum phase shift angle of 90°. The difference between the two powers is minimal as depicted in Fig. 6 which validate the analysis based on AC fundamental component. P_{2lit} is compared with real part of (7) or (8), P_2 with varying phase shift angle, α_2 to show the whole range of power level.

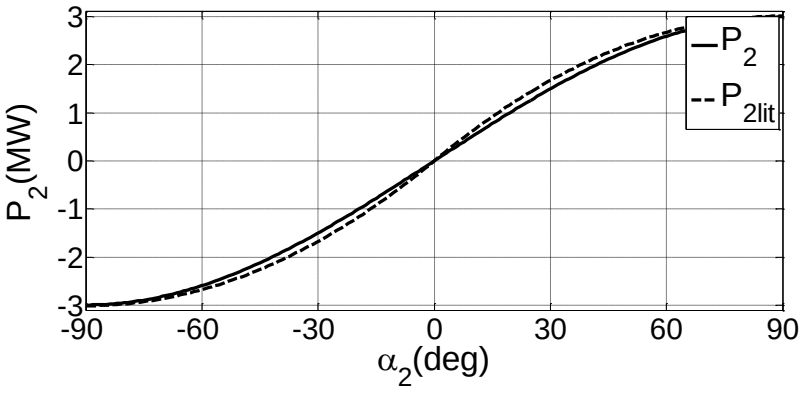
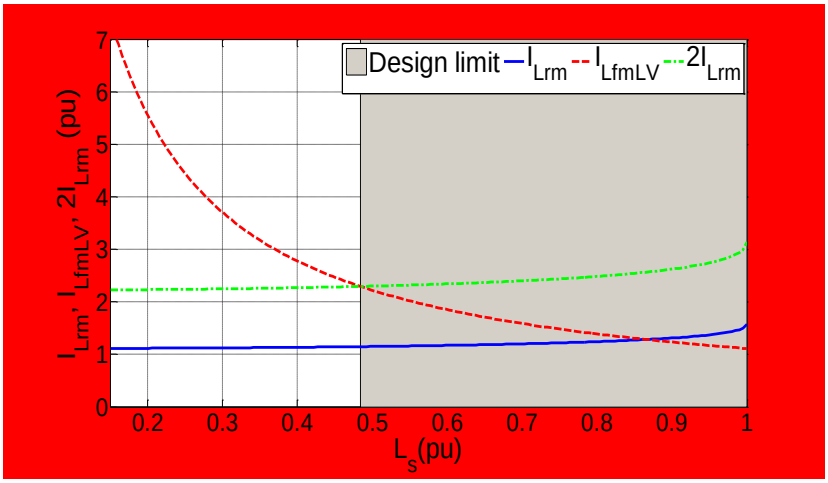
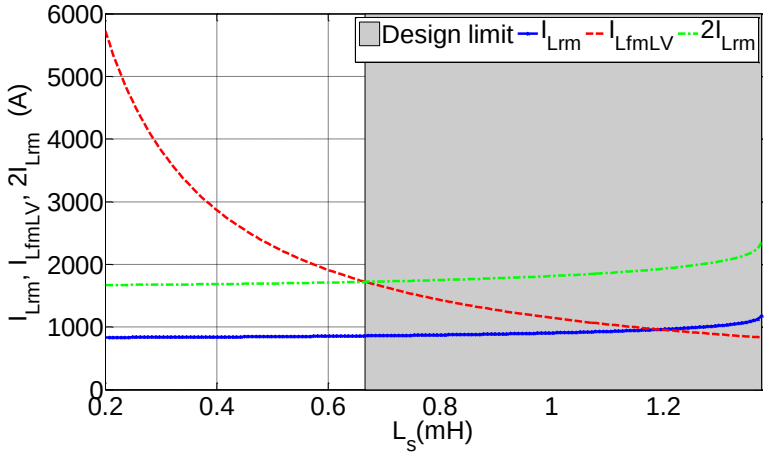


Fig. 6. Comparison of the power level using fundamental component analysis and literature [8]

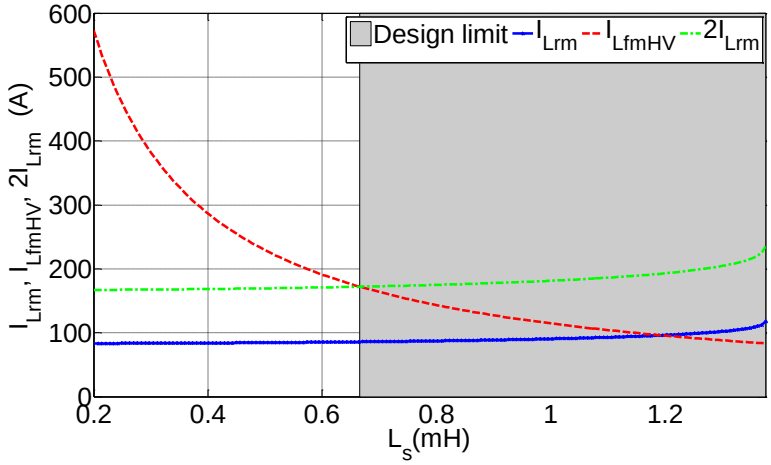
Fig. 7 shows the rated and fault current RMS magnitude for fault at LV and HV side terminals using (12) and (20), respectively. The design limit of two times the rated current is also included in Fig. 7 to give the design boundary for the DAB converter. The per unit plot is given in Fig. 7(a) where the value of L_s (pu) that the fault current magnitude exceeds the rated pu current magnitude is 0.866 pu while the set boundary of two times the rated pu current 0.48 pu. Below the set boundary limit, the fault current can significantly increase if no controller is realised. Based on the specification in Table I, the value of L_s that the fault current magnitude exceeds the rated current magnitude is 1.19 mH while the set boundary of two times the rated current magnitude is 0.67 mH for the LV and HV sides DC terminal fault are shown in Fig. 7(b) and Fig. 7(c), respectively.



(a)



(b)



(c)

Fig. 7. Rated and fault current RMS magnitude, (a) per unit value (b) LV side DC terminal fault (using Table I), (c) HV side DC terminal fault (using Table I)

IV. SIMULATION RESULTS

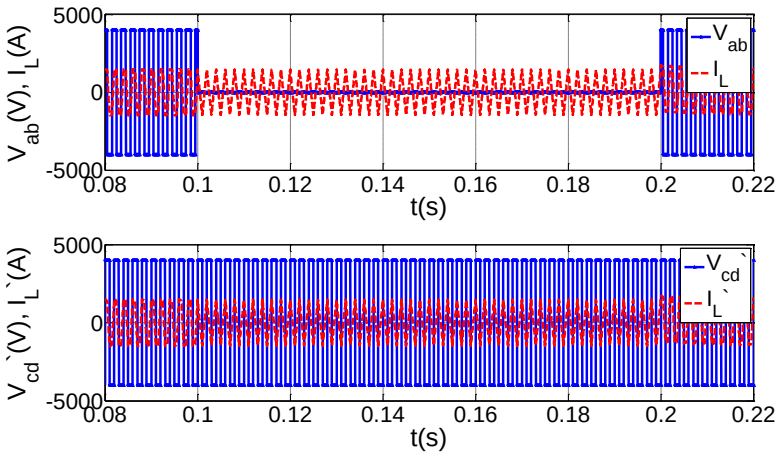
The DAB converter is simulated in MATLAB/Simulink. The specification of the DAB converter is in Table I. Simulation results for maximum phase shift angle of 90° are presented to confirm the theoretical part of the work. Therefore, the selected inductor for the simulation is 1.38 mH. The DC voltages are assumed to be fixed at its rated value unless DC fault is applied. DC Fault is applied at the DC terminal at *t*

= 0.1 second. Prior to fault, the converter is also assumed to be operating at full power and the power flow is from LV to HV side.

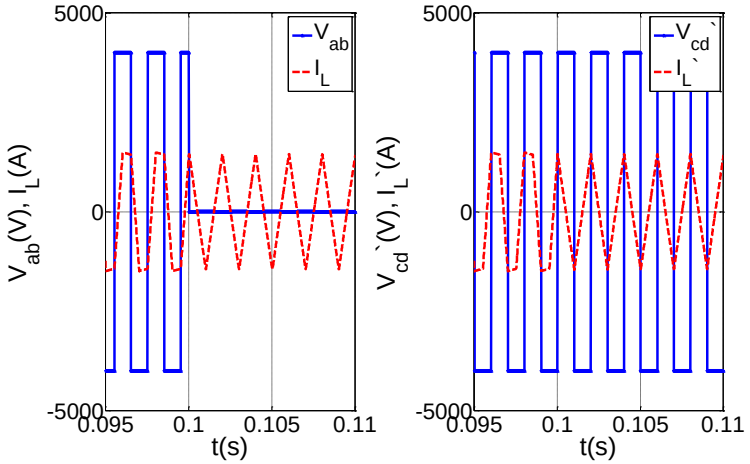
In Fig. 8, the AC voltages, v_{ab}, v_{cd} and inductor current, i_L are shown for the case of LV side faults (V_{dc1}=0). For the LV side, the actual simulated values are shown while for the HV sides, all the variables are referred to the LV side values. i_L is shown on for convenient to observed the waveform on LV and HV sides, but this value is similar. Zoom view of the AC voltages and inductor current during fault and after fault are given for better observations of the converter performance during fault. The RMS inductor current during steady state is approximately 1200 A. During fault, the RMS inductor current magnitude is 850 A. This value agrees with (17) which confirm that the converter is operating at lower RMS current during DC fault. Triangular waveform has smaller RMS value compare to sinusoidal and trapezoidal waveforms. The peak can also be observed from the zoom view to be similar as the steady state value.

During fault at HV (V_{dc2} = 0), the AC sides voltages and currents waveforms are shown in Fig. 9. In Fig. 9(b), the RMS fault current magnitude is observed to be at 850 A (similar to LV side fault because this is referred value). At the instant DC fault is applied, transient peak current is observed at 40% more than the steady-state current. Comparing to (22), the magnitude ratio of the fault current is observed to be 1.4 times more than the steady-state current. For this specific simulation, the overshoot is caused by the voltage across inductor ($v_L = v_{ab}$-v_{cd}') is high compare to fault at LV sides. This transient peak current gives non-zero average flux in the transformer which in turn can give DC offset to the AC current. However, the average current goes back to zero after 20 milliseconds fault is applied. Therefore, the saturation of the transformer core and semiconductor damage caused by the transient current is minimal. Additionally, the transformer is normally operated lower than the saturation flux density and for the semiconductor switches, it can withstand transient current pulse double of its rated value for few tenth of a second. For protection against this, controller shall be realized in the future.

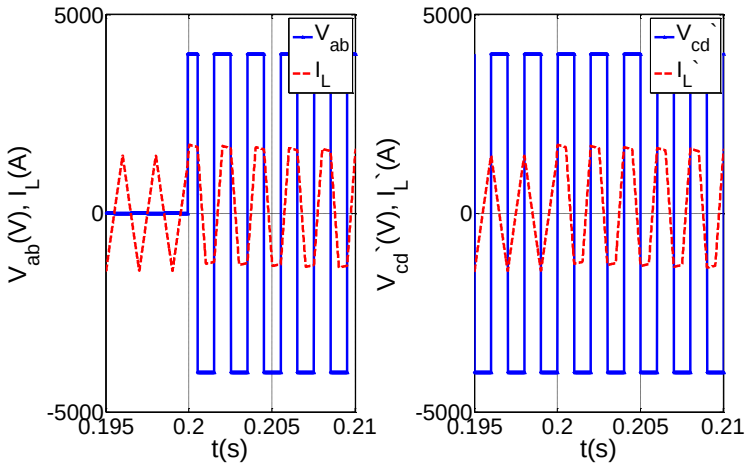
Both DC fault cases have RMS fault current magnitude shown in Fig. 8(d) and 9(d) shows similarity to the theoretical study value as depicted in Fig. 7. The converter shows good response when DC fault is applied and during fault recovery without any control actions. The performance of the DAB converter for reverse power (from HV to LV sides) is expected to be similar.



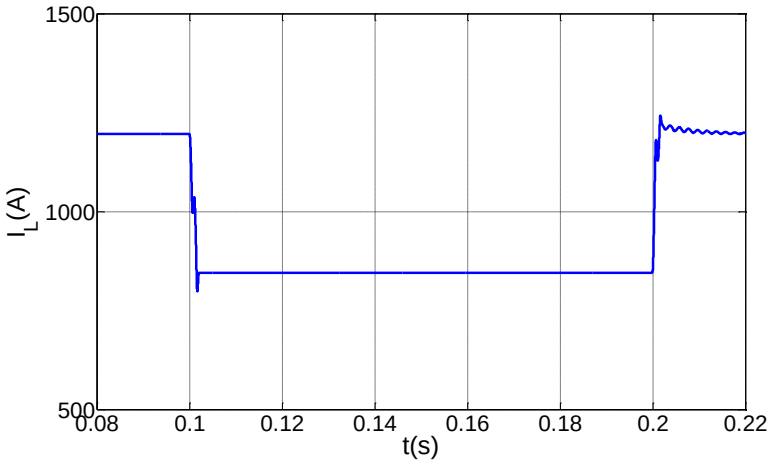
(a)



(b)

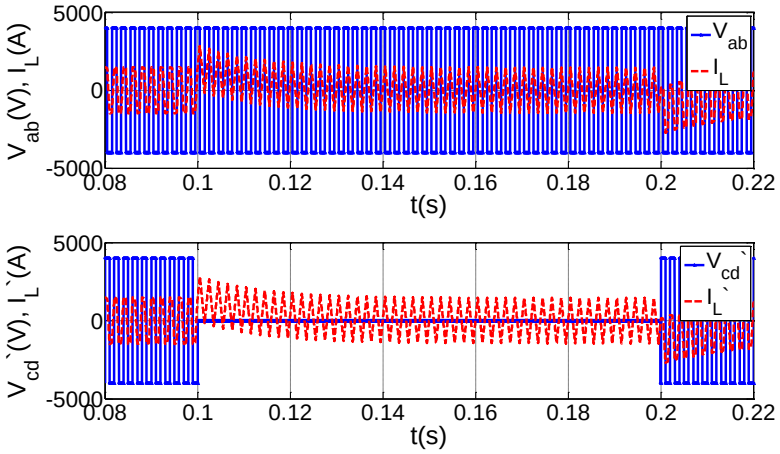


(c)

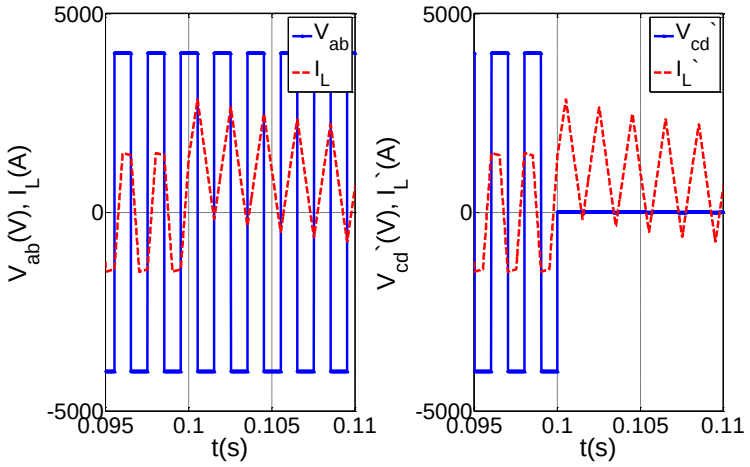


(d)

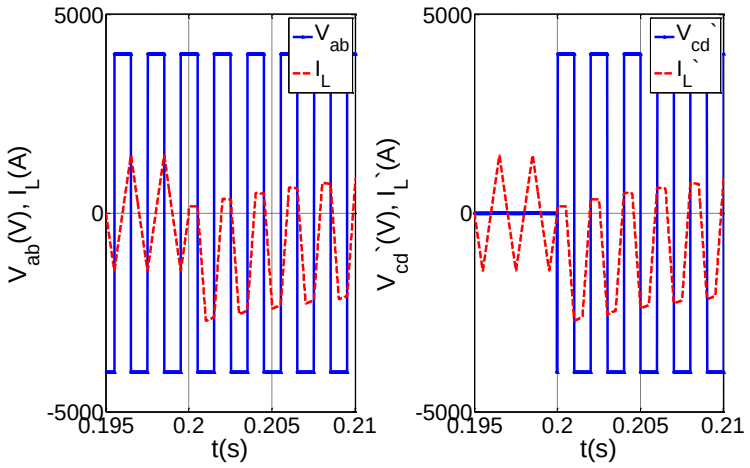
Fig. 8. Time domain simulation fault at LV DC terminal, (a) AC voltages and currents, (b) Zoom view during fault is applied, (c) Zoom view during fault recovery, (d) fundamental RMS inductor current magnitude


5000
0
-5000
0.08
0.1
0.12
0.14
0.16
0.18
0.2
0.22
t(s)
V_ab(V), I_L(A)
V_ab
I_L
V_cd`(V), I_L`(A)
V_cd`
I_L`

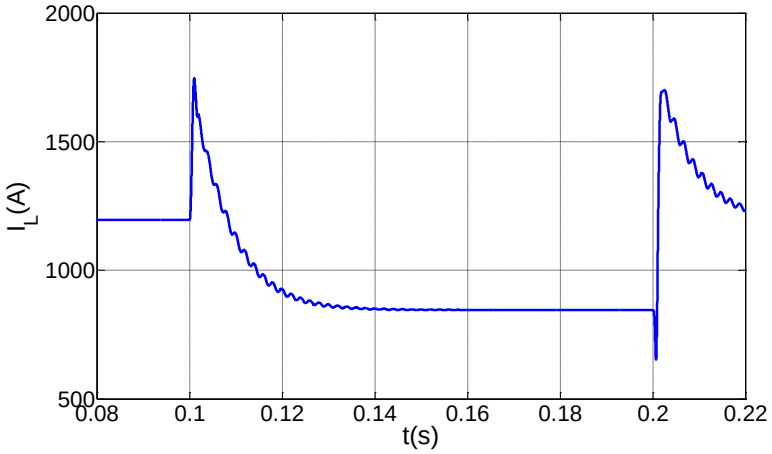
(a)


5000
0
-5000
0.095
0.1
0.105
0.11
t(s)
V_ab(V), I_L(A)
V_ab
I_L
V_cd`(V), I_L`(A)
V_cd`
I_L`

(b)


5000
0
-5000
0.195
0.2
0.205
0.21
t(s)
V_ab(V), I_L(A)
V_ab
I_L
V_cd`(V), I_L`(A)
V_cd`
I_L`

(c)



(d)

Fig. 9. Time domain simulation fault at HV DC terminal, (a) AC voltages and currents, (b) Zoom view during fault is applied, (c) Zoom view during fault recovery, (d) fundamental RMS inductor current magnitude

V. PROTOTYPE

A 500 W DAB prototype with 24/100V operating voltage is shown in Fig. 10. Table II shows the prototype specification of the DAB converter. IGBT switches with anti-parallel diodes from Semikron are used for the LV side switches while the HV side switches are from Fairchild Semiconductors. The MF transformer core for the DAB converter is from Magnetec GmbH and the windings are hand wound by the author. The converter is running at open loop control to validate the fault current studies and simulations work. The controller for the open loop control gate signals is DSP TMS320F28335 from Texas Instruments. The LV side DC terminal of the DAB is connected to a 24 V DC power supply whereas the HV side DC terminal is connected to a 100 V voltage source converter (VSC). Since DC power supply cannot sink current, a resistor is connected in parallel with the DC power supply to enable power to be sink. A power diode is also connected in series with the DC power supply to prevent the current to sink through the DC power supply.

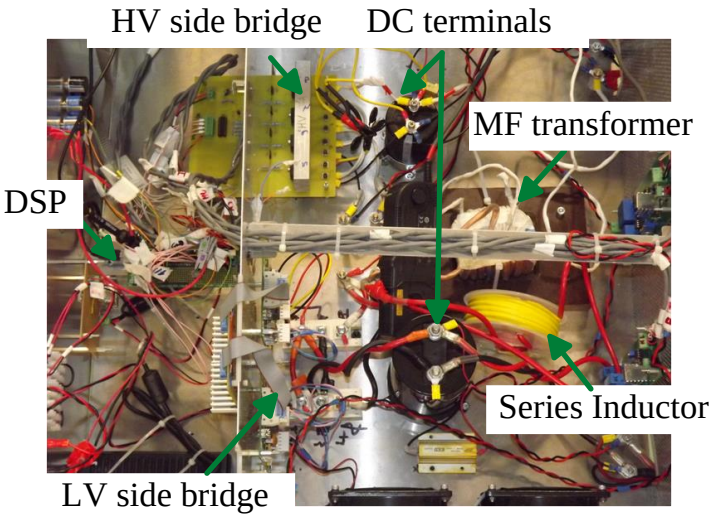


Fig. 10. 500 W prototype of the DAB DC/DC converter

Fig. 11 shows typical DAB converter waveform during steady-state operation. In this figure, the yellow waveform is the LV AC voltage, v_{ab}, the green waveform is the AC voltage at HV side, v_{cd}, the blue and red waveform is the inductor current (blue waveform are taken from the LV side and red waveform from the HV side).

TABLE II
SYSTEM PARAMETERS AT RATED VALUE

Parameters	Value
Power, P_1	500 W
DC voltage at LV, V_{dc1}	24 V
DC voltage at HV, V_{dc2}	100 V
Average DC current at LV, I_{dc1}	20.83 A
Average DC current at HV, I_{dc2}	5 A
Frequency, f	2000 Hz
Series plus leakage inductance	63.37 μH
LV side switches, SKM145GB174DN	170 V, 160 A
HV side switches, FGH80N60FD	600 V, 80 A
MF transformer (Nano-crystalline core)	16:67 turns

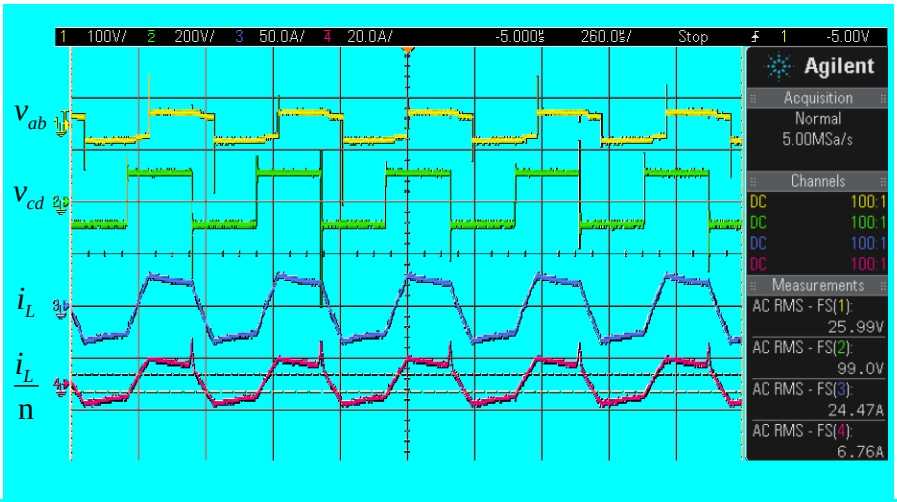
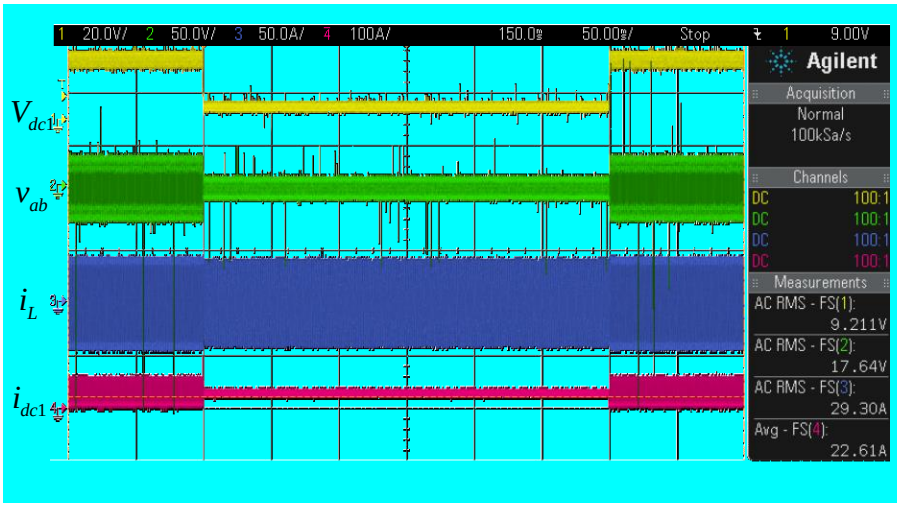
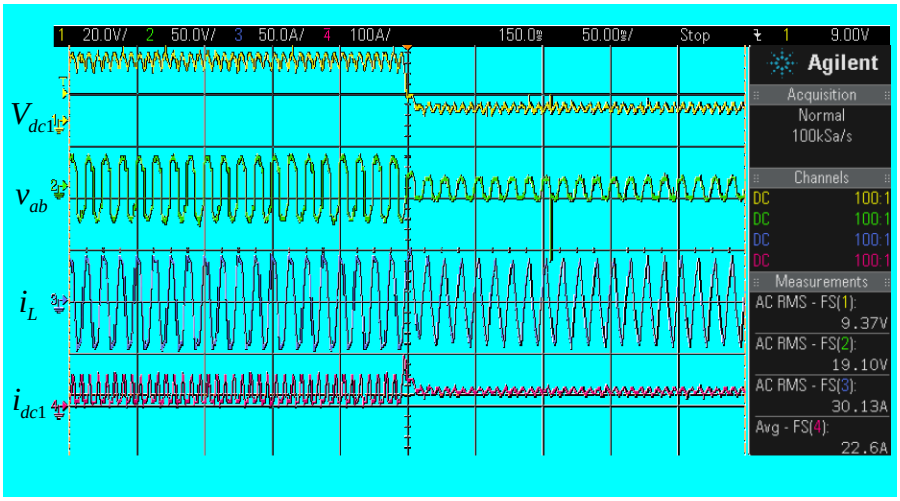


Fig. 11. Steady-state AC voltages and currents waveforms during normal conditions

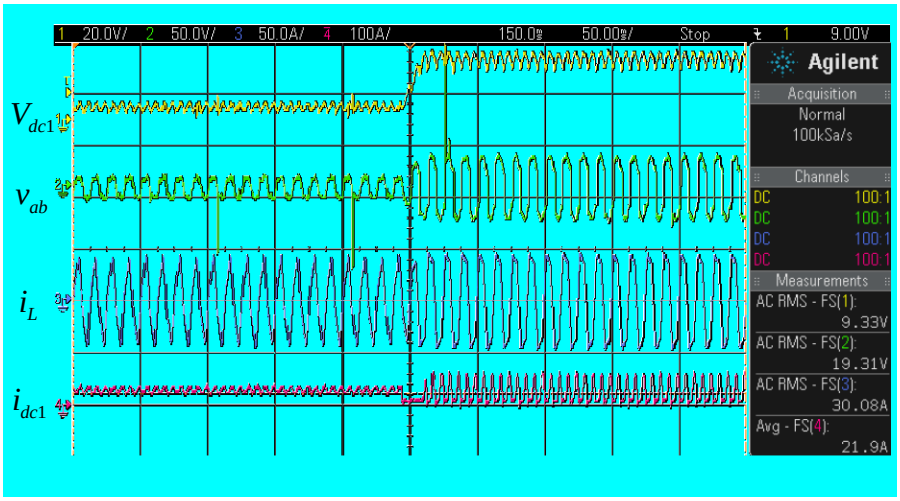
DC terminal fault is tested experimentally to verify the DAB converter capability and performance during fault. A DC fault hardware circuit is connected across the LV DC terminal. It is consists of power semiconductor device and power resistors used to short and direct fault current, respectively. DC fault is applied for 0.9 ms before fault recovery. Only DC fault at LV side is tested and enough to confirm the theoretical work. The waveform in Fig. 12 shows the LV side DC fault. The yellow waveform is the LV DC terminal voltage, V_{dc1}, the green waveform is the AC voltage at LV side, v_{ab}, the blue waveform is the inductor current, i_L and the red line is the DC current at LV side, I_{dc1}. During fault is applied, the converter performance is as expected (similar behaviour as simulation). No damaging current is observed. The peak value is also similar as analysed theoretically and as observed during simulations work. It can also be seen that the current waveform becomes triangular during fault. The peak current before and during DC fault has similar peak magnitude as expected. It is observed that the AC voltage, v_{ab} in Fig. 12(a) is non zero whereas in Fig. 8(a), v_{ab} is zero. This non zero voltage is the voltage across the design value of the fault hardware power resistors. However, this is sufficient to validate the DC fault capability of the converter.


1 20.0V/ 2 50.0V/ 3 50.0A/ 4 100A/ 150.0µs 50.00µs/ Stop 1 9.00V
Agilent
Acquisition
Normal
100kSa/s
Channels
DC 100:1
DC 100:1
DC 100:1
DC 100:1
Measurements
AC RMS - FS(1):
9.211V
AC RMS - FS(2):
17.64V
AC RMS - FS(3):
29.30A
Avg - FS(4):
22.61A
V_{dc1}
v_{ab}
i_L
i_{dc1}

(a)


1 20.0V/ 2 50.0V/ 3 50.0A/ 4 100A/ 150.0µs 50.00µs/ Stop 1 9.00V
Agilent
Acquisition
Normal
100kSa/s
Channels
DC 100:1
DC 100:1
DC 100:1
DC 100:1
Measurements
AC RMS - FS(1):
9.37V
AC RMS - FS(2):
19.10V
AC RMS - FS(3):
30.13A
Avg - FS(4):
22.6A
V_{dc1}
v_{ab}
i_L
i_{dc1}

(b)



(c)

Fig. 12. Practical results for the DAB 500 W prototype, (a) LV DC terminal fault for the, (b) During DC fault is apply (c) Recovery after DC fault

At the DC side current, a transient peak is observed during fault but this is within the capability of the switches transient (pulse current) specification. The fault recovery is as expected and it takes less than 100 μs for the converter to recover to its normal steady-state operation.

VI. CONCLUSION

This paper has introduced fault studies for DAB DC/DC converter based on its fundamental component of the AC voltages and currents. The fault currents were derived and simulated for DC terminal fault using MATLAB/Simulink. The performance of the converter was satisfactory during DC fault operation. The theoretical fault study has been confirmed by simulation and experimental works. This study concluded that the converter is capable to operate during faults even without any control action.

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